CLAIMS

What is claimed is:

1. A digital-to-analog converter (DAC), comprising:

a digital input;

a current-source element responsive to the digital input sourcing a current having a total current magnitude; and

a memory associated with the current-source element, wherein the total current magnitude sourced by said current source element is responsive to said memory.

2. A DAC in accordance with claim 1, wherein said total current magnitude comprises a first current magnitude and a second current magnitude, said first current magnitude being sourced by a first transistor and said second current magnitude being sourced by a second transistor.

3. A DAC in accordance with claim 2, wherein said second current magnitude is responsive to said memory and said first current magnitude is not.

4. A DAC in accordance with claim 3, wherein said first transistor includes a voltage input for controlling said first current magnitude.

5. A DAC in accordance with claim 1, wherein said memory is a nonvolatile memory.

6. A DAC in accordance with claim 5, wherein said memory is a nonvolatile memory.

7. . A DAC in accordance with claim 6, wherein said nonvolatile memory includes a floating gate for storing charge.

8. A DAC in accordance with claim 7, wherein said floating gate stores an analog charge value.

9. A DAC in accordance with claim 8 wherein said nonvolatile memory is the floating gate of a synapse transistor.

10. A DAC in accordance with claim 9 wherein said synapse transistor is a p-channel MOSFET.

11. A DAC in accordance with claim 9 wherein said synapse transistor includes a control-gate electrode.

12. A DAC in accordance with claim 9 wherein said synapse transistor does not have a control-gate electrode.

13. A digital-to-analog converter (DAC), comprising:

a codeword register receiving a digital codeword for conversion to an analog current signal;

a current-source responsive to a state of the codeword register;

a trim device coupled to the current-source, wherein the current-source and the trim device provide a combined current output, said trim device including a memory storing a trim weight used by the trim device to adjust said combined current output.

14. A DAC in accordance with claim 13, wherein said memory is a nonvolatile memory.

15. A DAC in accordance with claim 14, wherein said nonvolatile memory includes a floating gate for storing charge.

16. A DAC in accordance with claim 15, wherein said floating gate stores an analog charge value.

17. A DAC in accordance with claim 16 wherein said nonvolatile memory is the floating gate of a synapse transistor.

18. A DAC in accordance with claim 17 wherein said synapse transistor is a p-channel MOSFET.

19. A DAC in accordance with claim 17 wherein said synapse transistor includes a control-gate electrode.

20. A DAC in accordance with claim 17 wherein said synapse transistor does not have a control-gate electrode.

21. A trimmable current-source element for a current-steering-type digital-to-analog converter (DAC), said element comprising:

a first current-source transistor having a source and a drain and sourcing a first magnitude of current to an output node; and

a memory coupled to said first current-source transistor, said first magnitude of current responsive to said memory.

22. A trimmable current-source element in accordance with claim 21, wherein said memory is a nonvolatile memory.

23. A trimmable current-source element in accordance with claim 22, wherein said nonvolatile memory is a floating gate of said first current-source transistor.

24. A trimmable current-source transistor in accordance with claim 23, further comprising:

a tunneling device coupled to remove electrons from said floating gate in response to application of a tunneling control voltage to said tunneling device.

25. A trimmable current-source element in accordance with claim 24, further comprising:

an injector coupled to inject electrons onto said floating gate in response to application of an injection control voltage to said injector.

26. A trimmable current-source element in accordance with claim 21, further comprising:

a second current-source transistor having a source and a drain and sourcing a second magnitude of current to said output node, said output node providing a current comprising a sum of said first magnitude of current and said second magnitude of current.

27. A trimmable current-source element in accordance with claim 26, further comprising a reference voltage input to said second current-source transistor, said reference voltage input controlling said second magnitude of current.

28. A trimmable current-source element in accordance with claim 25, further comprising:

a second current-source transistor having a source and a drain and sourcing a second magnitude of current to said output node, said output node providing a current comprising a sum of said first magnitude of current and said second magnitude of current.

29. A trimmable current-source element in accordance with claim 28, further comprising a reference voltage input to said second current-source transistor, said reference voltage input controlling said second magnitude of current.

30. A trimmable current source element in accordance with claim 29, wherein said first current-source transistor is a synapse transistor.

31. A trimmable current-source element in accordance with claim 30, wherein said synapse transistor is a p-channel MOSFET.

32. A digital-to-analog converter (DAC), comprising

means for buffering a digital codeword for conversion to an analog current signal;

means for generating an output current at an output node responsive to a state of said buffering means;

means for trimming said output current, said trimming means including non-volatile memory means for controlling a current output of said trimming means.

33. A DAC in accordance with claim 32, wherein said nonvolatile memory means includes a floating gate for storing a charge.

34. A DAC in accordance with claim 33, further comprising means for erasing said floating gate.

35. A DAC in accordance with claim 34, wherein said erasing means includes a means for tunneling electrons off of said floating gate.

36. A pFET synapse transistor, comprising:

a p- doped substrate;

a first n- well and a second n- well disposed in said substrate;

a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;

a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;

a layer of gate oxide disposed above said channel, said first n- well and said second n- well;

a polysilicon floating gate disposed above said layer of gate oxide;

a source contact terminal electrically coupled to said source;

a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well.

37. A pFET synapse transistor in accordance with claim 36, wherein said third p+ doped region and said fourth p+ doped region are shorted together with a conductive layer which forms a bridge over said floating gate.

38. A pFET synapse transistor in accordance with claim 37, wherein said well contact terminal is strapped to said third p+ doped region and said fourth p+ doped region.

39. A pFET synapse transistor in accordance with claim 38, wherein said transistor is formed with a single layer of conductive polysilicon.

40. A pFET synapse transistor in accordance with claim 36 fabricated using a standard CMOS process.

41. A method for trimming a current-steering-type digital-to-analog converter (DAC), the DAC including an input codeword register and a plurality of trimmable current-source elements each having:

a current source transistor having a source and drain;

a trim device having a floating gate, a source and a drain, said source and drain of said trim device coupled in parallel with said source and drain of said current-source transistor;

an injection device coupled to inject electrons onto said floating gate in response to application of an injection control voltage to said injection device;

a tunneling device coupled to remove electrons from said floating gate in response to application of a tunneling control voltage to said tunneling device; and

an output node coupled to said drain of said current source transistor and said drain of said trim device; said method comprising:

erasing the floating gates of all trim devices by applying a relatively high tunneling control voltage to said tunneling devices; and

trimming each current-source element using electron injection by applying a negative voltage to each trim device's drain.

42. A method in accordance with claim 41, wherein said trimming includes:

comparing (1) a first total current generated by the DAC in response to a first codeword applied to the codeword register of the DAC added to the current from an additional LSB current-source with (2) a second total current generated by the DAC in response to a second codeword applied to the codeword register of the DAC, and trimming a current-source used to generate the second total current so that the second total current is substantially equal to the first total current.

43. A method in accordance with claim 42, wherein said comparing is performed sequentially for a plurality of the current-source elements with a single comparator.